PROCESS FOR MANUFACTURING A BYTE SELECTION TRANSISTOR FOR A MATRIX OF NON VOLATILE MEMORY CELLS AND CORRESPONDING STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a process for manufacturing a byte selection transistor for a matrix of non volatile memory cells and corresponding structure.

More specifically, the invention relates to a process for manufacturing a byte selection transistor for a matrix of non volatile memory cells organised in rows and columns integrated on a semiconductor substrate, each memory cell comprising a floating gate transistor and a selection transistor, the process providing the following steps:

defining on a same semiconductor substrate respective active areas for said byte selection transistor, for said floating gate transistor and for said selection transistor split by portions of insulating layer;

depositing a multilayer structure comprising at least a gate oxide layer, a first polysilicon layer, a dielectric layer on the whole substrate and a second polysilicon layer.

The invention relates also to a circuit structure comprising a matrix of non volatile memory cells organised in rows and columns integrated on a semiconductor substrate, associated to a circuitry comprising high and low voltage transistors, each memory cell comprising a floating gate transistor and a selection transistor, said rows being interrupted by at least a couple of byte selection transistors, said transistors being manufactured in respective active areas delimited by portions of insulating layer.

The invention relates particularly, but not exclusively, to a process for manufacturing a byte selection transistor for a matrix of non volatile memory cells and the following description is made with reference to this field of application for convenience of illustration only.

Description of the Related Art

As it is well known, a matrix of non volatile memory cells comprises a plurality of non volatile memory cells integrated on a semiconductor material substrate arranged in rows and columns.

Each non volatile cell is formed by a floating gate transistor and by a selection transistor. The floating gate region of the floating gate transistor is formed on a semiconductor substrate and split therefrom by a thin gate oxide layer. A control gate region is capacitively coupled to the floating gate region by means of a dielectric layer and metallic electrodes are provided to contact the drain, source terminals and the control gate region in order to apply predetermined voltage values to the memory cell. The selection transistor is instead manufactured by means of a traditional MOS transistor comprising a gate region formed on a semiconductor substrate and split therefrom by a thin gate oxide layer. Source and drain regions are integrated in the substrate at the gate region ends.

The cells belonging to a same word line have a common electric line driving the respective control gates by means of the byte selection transistor, while the cells belonging to a same bit line have common drain terminals.

The matrix of memory cells is organized in turn in bytes, each one comprising 8 bits (or multiples). Each byte can be selected from outside the matrix by means of a byte transistor located in correspondence with each byte.

A first known technical solution to form a matrix of non volatile cells provides the use of two different masks for manufacturing the selection and byte transistors having a gate region with a single polysilicon level, while the gate

region of the floating gate transistor is manufactured with a double polysilicon layer.

Therefore, in the matrix portion wherein the selection and byte transistors are manufactured a removal step of one of the two polysilicon layers used to form the double polysilicon layer must be performed.

Although advantageous under many aspects, this first solution has several drawbacks. In fact, the removal step of a polysilicon layer from the active areas of the selection and byte transistors of one of the two polysilicon layers can degrade the electric features of these devices. Moreover the resulting structure comprises the series of devices with different heights which make the cleaning steps provided in the traditional process flow particularly difficult.

SUMMARY OF THE INVENTION

According to principles of the present invention a process is described for manufacturing a byte transistor integrated in a matrix of non volatile memory cells, having such structural and functional features as to allow the number of masks to be used in the manufacturing process to be reduced overcoming the limits and/or drawbacks still affecting prior art devices.

The solution idea underlying the present invention is to form the gate region of the byte selection transistor using the same two overlapped layers which are used for the gate regions of the selection transistor and for the gate regions of the floating gate transistor and to form the electric connection between these two polysilicon layers near the byte transistor.

The features and advantages of the device according to the invention will be apparent from the following description of an embodiment thereof given by way of non-limiting example with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In these drawings:

Figure 1 shows a simplified diagram of a wiring diagram of a matrix of non volatile memory cells comprising bit and byte selection transistors;

Figure 2 shows a magnification of a portion A of the matrix of cells of figure 1 comprising a byte selection transistor according to the invention;

Figure 3 is a sectional view along the line I-I of figure 2 of a traditional memory cell;

Figures 4 and 5 are sectional views along the line II-II of a matrix portion of figure 2 during the two different steps of the manufacturing process.

DETAILED DESCRIPTION OF THE INVENTION

With reference to these drawings, a process for manufacturing a byte selection transistor for a matrix of non volatile memory cells is described.

The present invention can be implemented together with other integrated circuit manufacturing techniques presently used and well known in this field, therefore only those commonly used process steps which are necessary to understand the present invention are included together with the description of the invention.

The figures representing cross sections of integrated circuit portions during the manufacturing are not drawn to scale, but they are instead drawn in order to show the most important features of the invention.

With reference to figures 1-3, a thick oxide layer 2 is selectively formed, for example grown, on a semiconductor substrate in order to form active areas 3 wherein the non volatile memory cells 5 are respectively formed, each one comprising a floating gate transistor 6 and a selection transistor 7 and byte selection transistors 8. The oxide layer 2 can also be a trench or other isolation structure.

As shown in figure 3, a second oxide layer 9 of a first thickness to form the gate oxides of the floating gate transistor 6, of the selection transistor 7 and of the byte selection transistor 8. In some embodiments, a third oxide layer 10

of a second thickness being less than the thickness of the second layer 9 to form the tunnel oxide of the floating gate transistor 6 are selectively formed.

Traditionally, in this process step the gate oxide layer of high voltage transistors comprised in the matrix control circuitry, not shown in the drawings, is also formed by means of the second oxide layer 9.

A layered structure is then formed on the whole substrate 1 comprising a first polysilicon layer 11, a fourth dielectric layer 12 called interpoly oxide and a second polysilicon layer 13.

This fourth dielectric layer 12 is for example an ONO (Oxide-Nitride-Oxide) layer.

Advantageously, in this process step after depositing the fourth dielectric layer 12 called interpoly oxide a fifth oxide layer is also formed, to form the gate oxide layer of low voltage transistors which can be used to manufacture other types of memory devices on the same substrate 1, such as for example ROM or SDRAM memories, and the devices implementing the matrix control logic, non shown in the drawings.

Advantageously, by forming this fifth oxide layer last, the devices implementing the low voltage control logic are manufactured with a manufacturing process not depending on the process used for the memory matrix and high voltage devices. It is thus possible to perform an optimisation of manufacturing process parameters of single devices.

This layered structure is selectively removed, as shown in figure 2, by means of a photolithographic process providing the use of a mask called "of the self-aligned etching", to form simultaneously the gate regions of the floating gate transistor 6, of the selection transistor 7 and of the byte selection transistor 8.

Two bands S1 and S2 are thus formed on the substrate 1. The band S1 in correspondence with the respective active areas 3 of the selection transistor 7 and of the byte selection transistor 8 forms the respective gate regions thereof,

while the band S2 in correspondence with the respective active areas 3 of the floating gate transistor 6 forms the respective gate regions thereof.

According to the invention, the band S1 extends over the byte transistor 8 on the oxide layer 2 in order to form a pad 4.

This pad 4 is used to put the first polysilicon layer 11 in contact with the second polysilicon layer 13.

Advantageously, the width WI of the pad 4 is greater than the width W2 of the portion S1 which forms the gate regions of transistors 7 and 8.

In other words, the band S1 has an enlarged portion between adjacent byte selection transistors.

In particular, as shown in greater detail in figures 4 and 5, according to the invention an opening 4a exposing the dielectric layer 12 is formed in the second polysilicon layer 13 having a width W3 within said pad 4.

This dielectric layer 12 is then removed through the opening 4a formed in the second polysilicon layer 13.

Advantageously, this opening 4a is formed in the same process step in which the gate regions of transistors of the low voltage circuitry associated to the matrix are manufactured.

At this point the process continues with the dopant implantation steps provided by the traditional process flow to form the junctions of matrix transistors.

Advantageously, the process then continues with the formation of a metal layer 14 on the whole substrate 1 surface. A thermal treatment is then performed to let the metal layer react with the substrate 1 surface and with the polysilicon layers 11 and 13 which are not covered by dielectric to form a silicide layer.

During the thermal treatment the transition metal only reacts with that substrate 1 portion not comprising an oxide layer. Therefore the second polysilicon layer 13 and the portion of the first polysilicon layer 11 exposed through the opening 4a are thus covered by a low resistance layer.

The interconnection lines used in the matrix of cells are formed at this stage. In particular, a conductive layer 15 is formed in the opening 4a formed in the second polysilicon layer 13 in order to fill at least partially said opening 4a. The conductive layer 15 puts the first polysilicon layer 11 in electrical contact with the second polysilicon layer 13, as shown in figure 5.

Advantageously, a portion 15a of the conductive layer 15 can be formed in other to locations, for example, to put a junction of the byte selection transistor 8 in contact with the gate region of the floating gate transistor 6 of the memory cell 5.

The conductive layer 15 can be a further polysilicon layer or a metallization layer.

The circuit structure according to the invention is now described, comprising a matrix of non volatile memory cells, for example of the EEPROM type. This matrix comprises a plurality of non volatile memory cells 5 integrated on a semiconductor material substrate 1 arranged in rows, or word lines W, ..., WLn, WLn+1 and columns or bit lines B0, ..., BL7, as shown in figure 1. Traditionally, a dummy reference column BL is between two adjacent bytes.

Each non volatile cell 5 is formed by a floating gate transistor 6 and by a selection transistor 7. The floating gate region of the floating gate transistor 6 is formed on a semiconductor substrate 1 and split therefrom by means of a gate oxide layer 9. A control gate region is capacitively coupled to the floating gate region by means of a dielectric layer and metallic electrodes are provided to contact the drain, source terminals and the control gate region, for example CGn, GCn+1, in order to apply predetermined voltage values to the memory cell.

The cells 5 belonging to a same word line have a common electric line driving the respective control gate regions by means of the byte selection transistor 7, while the cells 5 belonging to a same bit line have common drain terminals.

Also the control circuitry of the matrix of memory cells traditionally comprising high voltage transistors to handle the signals in the matrix of memory cells is integrated on the same substrate 1.

The matrix of memory cells is organized in turn in bytes B, each one comprising 8 bits (or multiples). Each byte can be selected from outside the matrix by means of a byte selection transistor 8 located in correspondence with each byte. Each byte selection transistor 8 is formed in a corresponding active area 3 delimited by a thick oxide layer 2.

According to the invention, the gate regions of floating gate transistors, of selection transistors and of byte selection transistors are formed by means of a multilayer structure formed on the semiconductor substrate 1 comprising a first oxide layer 9, a first polysilicon layer 11, a second oxide layer 12 and a second polysilicon layer 13. In particular, this multilayer structure comprises a first band S1 common to all selection transistors 7 belonging to the same byte and to the relevant byte selection transistor 8 and a second band S2 common to all floating gate transistor 6 belonging to the same byte. A portion 4 of this band S1 also extends on the thick oxide layer 2 delimiting the active area 3 of the byte selection transistor 8.

In particular, the band S1 in correspondence with the respective active areas 3 of the selection transistor 7 and of the byte selection transistor 8 forms the respective gate regions thereof, while the band S2 in correspondence with the respective active areas 3 of the floating gate transistor 6 forms the respective gate regions thereof.

Advantageously, the portion 4 can have a higher amplitude than the portion of the band S1 forming the gate regions of selection transistors and of the byte selection transistors in correspondence with the active areas 3 of these transistors 7, 8. In fact this portion 4 can have the pad 4 shape.

The second dielectric layer 12 and the second polysilicon layer 13 are provided with an opening 4a in correspondence with this pad 4.

Advantageously, the second polysilicon layer 13 and the portion of the first polysilicon layer 11 exposed through the opening 4a is covered by a low resistivity layer such as for example a silicide layer.

According to the invention, a conductive layer 15 fills at least partially the opening 4a forming the electric connection between the first and second polysilicon layers.

In conclusion, with the process according to the invention a particularly compact circuit structure is obtained, since the pad 4, which is used to put the two polysilicon layers forming the gate regions of selection transistors 7, 8 in electric contact and thus ensure the correct operation of these devices, is formed between two byte selection transistors 8 belonging to two adjacent bytes. The distance provided between two adjacent byte selection transistors 8 is selected in order to reduce the formation of parasite transistors between these two adjacent transistors which have to handle high voltages.

The further advantage of the present invention is to manufacture transistors in the matrix with a same number of polysilicon layers in order to facilitate the etching and selective removal steps being necessary during the manufacturing process steps. Forming all gate regions in the same process step considerably improves the reliability of the so-formed devices.

Advantageously, the circuit structure according to the invention allows very compact devices to be manufactured, such as for example SmartCard products, or devices which can be used in mobile telephony applications which must have a low voltage interface with the outside. Traditionally, the driving of the memory matrix in the circuit structure according to the invention is instead handled by high voltage transistors.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.